

IN THE CLAIMS

Please cancel Claim 4 without prejudice and amend Claims 1 and 2 as shown in marked-up form as follows:

1. (Currently Amended) Method of testing an electronic circuit device that comprises a first and second contact terminal and a first and second transistor with ~~main~~-current channels connected in parallel between the contact terminals, the method comprising
    - connecting a first and second sense contact of a resistance measuring device to the first and second terminal respectively;
    - bringing the electronic circuit into a first, second and third state respectively, the first and second transistor being switched on and off respectively in the first state and vice versa in the second state, both transistors being switched on in the third state;
    - measuring a first, second and third resistance value of a resistance between the first and second sense contact with the resistance measuring device in the first, second and third state respectively;
    - computing a model resistance composed of a series resistance component in series with a parallel arrangement of a first and second resistance component, through the ~~main~~-current channel of
- S:\WX\Amendments\2003 Amendments\NL000229.amd2.rvsfmt.doc

the first and second transistor respectively from the first, second and third resistance value;

- performing a comparison which verifies whether a resistance measured by the resistance measuring device from which the series component has been eliminated exceeds a threshold;
- rejecting the electronic circuit if the comparison indicates that the threshold is exceeded.

2. (Currently Amended) An electronic circuit device comprising:

a first and second contact terminal;

a first and second switching transistor each with a main current channel, the ~~main~~-current channels being coupled in parallel between the first and second contact terminal, both for substantially providing a switchable short-circuit between the first and second contact terminal though the main current channels in a normal operating mode;

a control circuit, the control circuit being arranged to switch the first and second switching transistors between at least three states, the first and second transistor being switched on and off respectively in the first state and vice versa in the second state, both transistors being switched on in the third state, wherein the switching transistor has only two contact terminals.

3. (Previously Amended) The electronic circuit device according to Claim 2, wherein the control circuit being switchable between the normal operating mode and a test operating mode, the control circuit switched the device to the first and second state in a test operating mode only.

4. (Withdrawn)